UBA2014

600 V driver IC for HF fluorescent lamps

Rev. 02 — 12 September 2005

Product data sheet

1. General description

The IC is a monolithic integrated circuit for driving electronically ballasted fluorescent lamps, with mains voltages up to 277 V (RMS) (nominal value).

The circuit is made in a 650 V Bipolar CMOS DMOS (BCD) power-logic process. It provides the drive function for the two discrete power MOSFETs.

Besides the drive function, the IC also includes the level-shift circuit, the oscillator function, a lamp voltage monitor, a current control function, a timer function and protections.

2. Features

- Adjustable preheat time
- Adjustable preheat current
- Current controlled operating
- Single ignition attempt
- Adaptive non-overlap time control
- Integrated high-voltage level-shift function
- Power-down function
- Protection against lamp failures or lamp removal
- Capacitive mode protection

3. Applications

- The circuit topology enables a broad range of ballast applications at different mains voltages for driving lamp types from T8, T5, PLC, T10, T12, PLL and PLT, for example.

4. Quick reference data

Table 1: Quick reference data

V_{DD} = 13 V; $V_{FVDD} - V_{SH}$ = 13 V; T_{amb} = 25 °C; all voltages are referenced to GND; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up state						
$V_{DD(start)}$	oscillator start supply voltage		12.4	13.0	13.6	V
$V_{DD(stop)}$	oscillator stop supply voltage		8.6	9.1	9.6	V
$I_{DD(start)}$	oscillator start-up supply current	$V_{DD} < V_{DD(start)}$	-	170	200	µA
High-voltage supply						
V_{HS}	high-side supply voltage	I_{HS} < 30 µA; t < 1 s	-	-	600	V
Reference voltage						
V_{VREF}	reference voltage	I_L = 10 µA	2.86	2.95	3.04	V
Voltage controlled oscillator						
f_{max}	maximum bridge frequency		90	100	110	kHz
f_{min}	minimum bridge frequency		38.9	40.5	42.1	kHz
High-side output driver						
$I_{o(source)}$	output source current	$V_{GH} - V_{SH}$ = 0 V	135	180	235	mA
$I_{o(sink)}$	output sink current	$V_{GH} - V_{SH}$ = 13 V	265	330	415	mA
Preheat current sensor						
V_{ph}	preheat voltage		0.57	0.60	0.63	V
Lamp voltage sensor						
$V_{lamp(fail)}$	lamp fail voltage		0.77	0.81	0.85	V
$V_{lamp(max)}$	maximum lamp voltage		1.44	1.49	1.54	V
Average current sensor						
V_{offset}	offset voltage	V_{CS} = 0 V to 2.5 V	–2	0	+2	mV
g_m	transconductance	f = 1 kHz	1900	3800	5700	µA/mV
Preheat timer						
t_{ph}	preheat time	C_{CT} = 330 nF; R_{IREF} = 33 kΩ	1.6	1.8	2.0	s
V_{OL}	LOW-level output voltage		-	1.4	-	V
V_{OH}	HIGH-level output voltage		-	3.6	-	V

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
UBA2014T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
UBA2014P	DIP16	plastic dual in-line package; 16 leads (300 mm); long body	SOT38-1

6. Block diagram

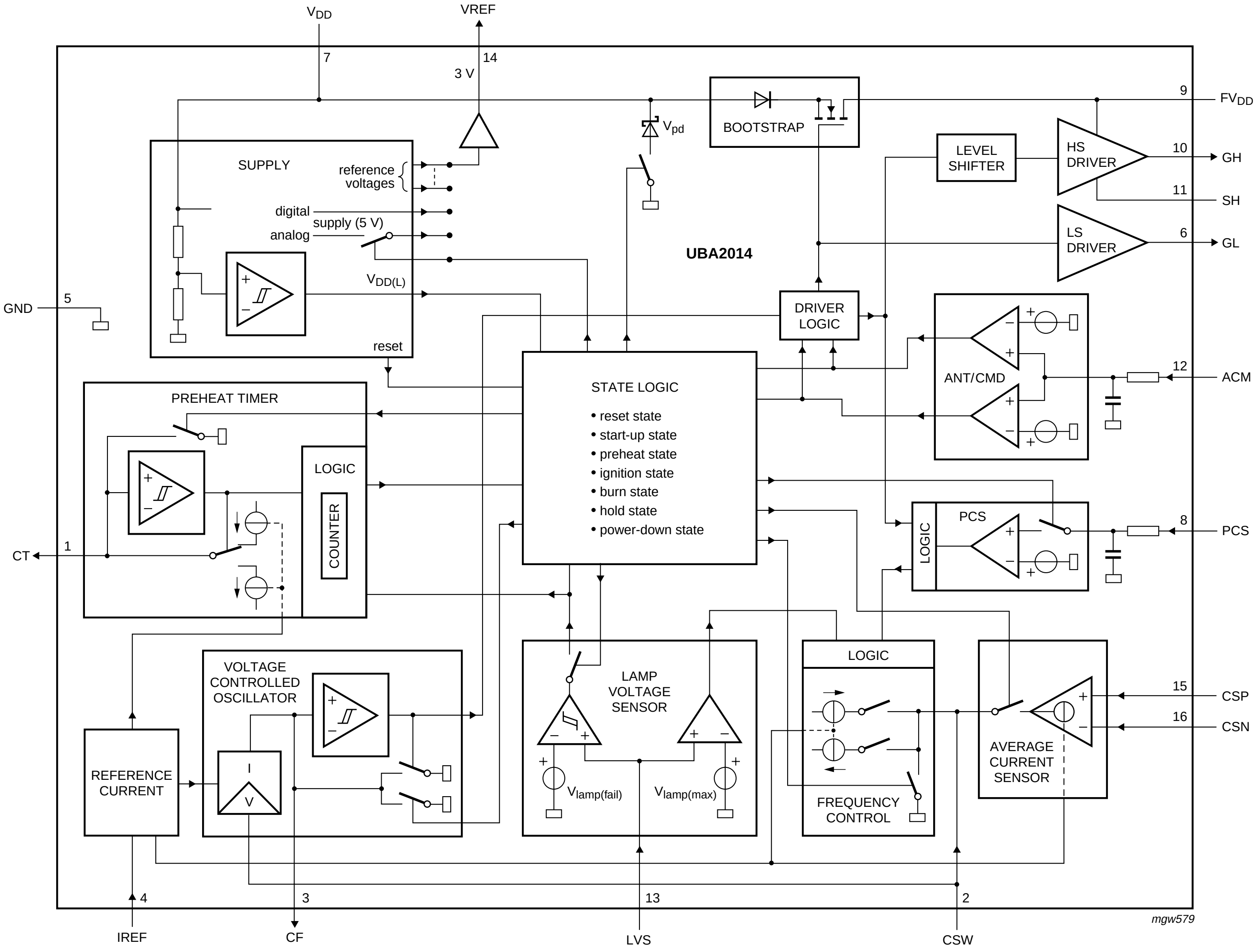


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

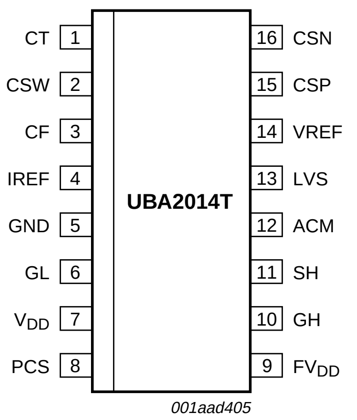


Fig 2. Pin configuration (SO16)

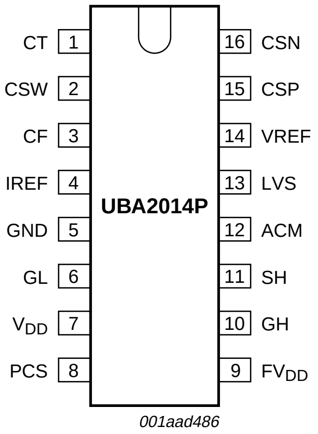


Fig 3. Pin configuration (DIP16)

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
CT	1	preheat timer output
CSW	2	input of voltage controlled oscillator
CF	3	voltage controlled oscillator output
IREF	4	internal reference current input
GND	5	ground
GL	6	gate output for the low-side switch
V_{DD}	7	low-voltage supply
PCS	8	preheat current sensor input
FV_{DD}	9	floating supply voltage; supply for high-side switch
GH	10	gate output for the high-side switch
SH	11	source for the high-side switch
ACM	12	capacitive mode input
LVS	13	lamp voltage sensor input
VREF	14	reference voltage output
CSP	15	positive input for the average current sensor
CSN	16	negative input for the average current sensor

8. Functional description

8.1 Start-up state

Initial start-up can be achieved by charging the low-voltage supply capacitor C7 (see Figure 8) via an external start-up resistor. Start-up of the circuit is achieved under the condition that both half-bridge transistors TR1 and TR2 are non-conductive. The circuit will be reset in the start-up state. If the low-voltage supply (V_{DD}) reaches the value of $V_{DD(start)}$ the circuit will start oscillating. A DC reset circuit is incorporated in the High-Side (HS) driver. Below the lock-out voltage at the FV_{DD} pin the output voltage ($V_{GH} - V_{SH}$) is zero. The voltages at pins CF and CT are zero during the start-up state.

8.2 Oscillation

The internal oscillator is a Voltage Controlled Oscillator (VCO) circuit which generates a sawtooth waveform between the $V_{CF(high)}$ level and 0 V. The frequency of the sawtooth is determined by capacitor C_{CF}, resistor R_{IREF}, and the voltage at pin CSW. The minimum and maximum switching frequencies are determined by R_{IREF} and C_{CF}; their ratio is internally fixed. The sawtooth frequency is twice the half-bridge frequency. The UBA2014 brings the transistors TR1 and TR2 into conduction alternately with a duty cycle of approximately 50 %. An overview of the oscillator signal and driver signals is illustrated in Figure 4. The oscillator starts oscillating at f_{max}. During the first switching cycle the Low-Side (LS) transistor is switched on. The first conducting time is made extra long to enable the bootstrap capacitor to charge.

8.3 Adaptive non-overlap

The non-overlap time is realized with an adaptive non-overlap circuit (ANT). By using an adaptive non-overlap circuit, the application can determine the duration of the non-overlap time and make it optimum for each frequency; see Figure 4. The non-overlap time is determined by the slope of the half-bridge voltage, and is detected by the signal across resistor R16 which is connected directly to pin ACM. The minimum non-overlap time is internally fixed. The maximum non-overlap time is internally fixed at approximately 25 % of the bridge period time. An internal filter of 30 ns is included at the ACM pin to increase the noise immunity.

8.4 Timing circuit

A timing circuit is included to determine the preheat time and the ignition time. The circuit consists of a clock generator and a counter.

The preheat time is defined by C_{CT} and R_{IREF} and consists of 7 pulses at C_{CT}; the maximum ignition time is 1 pulse at C_{CT}. The timing circuit starts operating after the start-up state, as soon as the low supply voltage (V_{DD}) has reached $V_{DD(start)}$ or when a critical value of the lamp voltage ($V_{lamp(fail)}$) is exceeded. When the timer is not operating C_{CT} is discharged to 0 V at 1 mA.

8.5 Preheat state

After starting at f_{max}, the frequency decreases until the momentary value of the voltage across sense resistor R14 reaches the internally fixed preheat voltage level (pin PCS). At crossing the preheat voltage level, the output current of the Preheat Current Sensor (PCS) circuit discharges the capacitor C_{CSW}, thus raising the frequency. The preheat time begins at the moment that the circuit starts oscillating. During the preheat time the Average Current Sensor (ACS) circuit is disabled. An internal filter of 30 ns is included at pin PCS to increase the noise immunity.

8.6 Ignition state

After the preheat time the ignition state is entered and the frequency will sweep down due to charging of the capacitor at pin CSW with an internally fixed current; see Figure 5. During this continuous decrease in frequency, the circuit approaches the resonant frequency of the load. This will cause a high voltage across the load, which normally ignites the lamp. The ignition voltage of a lamp is designed above the $V_{lamp(fail)}$ level. If the lamp voltage exceeds the $V_{lamp(fail)}$ level the ignition timer is started.

8.7 Burn state

If the lamp voltage does not exceed the $V_{lamp(max)}$ level the voltage at pin CSW will continue to increase until the clamp level at pin CSW is reached; see Figure 5. As a consequence the frequency will decrease until the minimum frequency is reached.

When the frequency reaches its minimum level it is assumed that the lamp has ignited and the circuit will enter the burn state. The Average Current Sensor (ACS) circuit will be enabled. As soon as the averaged voltage across sense resistor R14, measured at pin CSN, reaches the reference level at pin CSP, the average current sensor circuit will take over the control of the lamp current. The average current through R14 is transferred to a voltage at the voltage controlled oscillator and regulates the frequency and, as a result, the lamp current.

8.8 Lamp failure mode

8.8.1 During ignition state

If the lamp does not ignite, the voltage level increases. When the lamp voltage exceeds the $V_{lamp(max)}$ level, the voltage will be regulated at the $V_{lamp(max)}$ level; see Figure 6. When the $V_{lamp(fail)}$ level is crossed the ignition timer has already started. If the voltage at pin LVS is above the $V_{lamp(fail)}$ level at the end of the ignition time the circuit stops oscillating and is forced into the Power-down mode. The circuit will be reset only when the supply voltage is powered down.

8.8.2 During burn state

If the lamp fails during normal operation, the voltage across the lamp will increase and the lamp voltage will exceed the $V_{lamp(fail)}$ level; see Figure 7. At that moment the ignition timer is started. If the lamp voltage increases further it will reach the $V_{lamp(max)}$ level. This forces the circuit to re-enter the ignition state and results in an attempt to re-ignite the lamp. If during restart the lamp still fails, the voltage remains high until the end of the ignition time. At the end of the ignition time the circuit stops oscillating and the circuit will enter the Power-down mode.

8.9 Power-down mode

The Power-down mode will be entered if, at the end of the ignition time, the voltage at pin LVS is above $V_{lamp(fail)}$. In the Power-down mode the oscillator will be stopped and both TR1 and TR2 will be non-conductive. The V_{DD} supply is internally clamped. The circuit is released from the Power-down mode by lowering the low-voltage supply below $V_{DD(reset)}$.

8.10 Capacitive mode protection

The signal across R16 also gives information about the switching behavior of the half bridge. If, after the preheat state, the voltage across the ACM resistor (R16) does not exceed the V_{CMD} level during the non-overlap time, the Capacitive Mode Detection circuit (CMD) assumes that the circuit is in the capacitive mode of operation. As a consequence the frequency will directly be increased to f_{max}. The frequency behavior is decoupled from the voltage at pin CSW until C_{CSW} has been discharged to zero.

8.11 Charge coupling

Due to parasitic capacitive coupling to the high voltage circuitry all pins are burdened with a repetitive charge injection. Given the typical application the pins IREF and CF are sensitive to this charge injection. For charge coupling of approximately 8 pC, a safe functional operation of the IC is guaranteed, independent of the current level.

Charge coupling at current levels below 50 µA will not interfere with the accuracy of the V_{CS}, V_{PCS} and V_{ACM} levels.

Charge coupling at current levels below 20 µA will not interfere with the accuracy of any parameter.

8.12 Design equations

The following design equations are used to calculate the desired preheat time, the maximum ignition time, and the minimum and the maximum switching frequency.

$$t_{ph} = 1.8 \times \frac{C_{CT}}{330 \times 10^{-9}} \times \frac{R_{IREF}}{33 \times 10^{3}} \tag{1}$$

$$t_{ign} = 0.26 \times \frac{C_{CT}}{330 \times 10^{-9}} \times \frac{R_{IREF}}{33 \times 10^{3}} \tag{2}$$

$$f_{min} = 40.5 \times 10^{3} \times \frac{100 \times 10^{-12}}{C_{CF}} \times \frac{33 \times 10^{3}}{R_{IREF}} \tag{3}$$

$$f_{max} = 2.5 \times f_{min} \tag{4}$$

Start of ignition is defined as the moment at which the measured lamp voltage crosses the $V_{lamp(fail)}$ level; see Section 8.8.

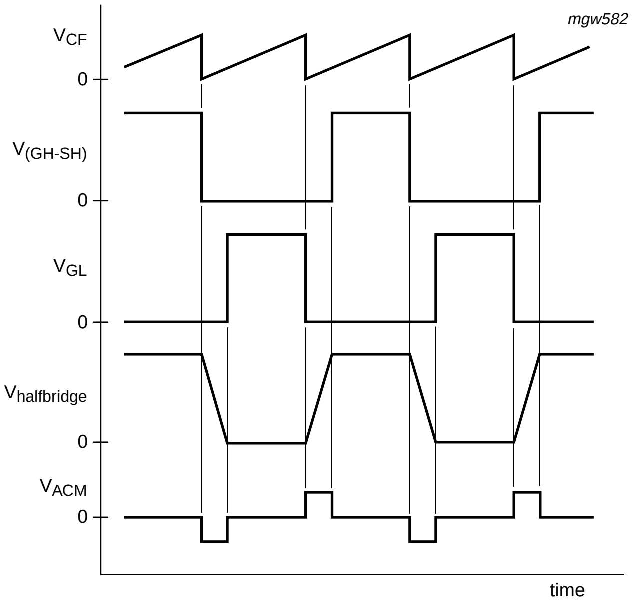


Fig 4. Oscillator and driver signals

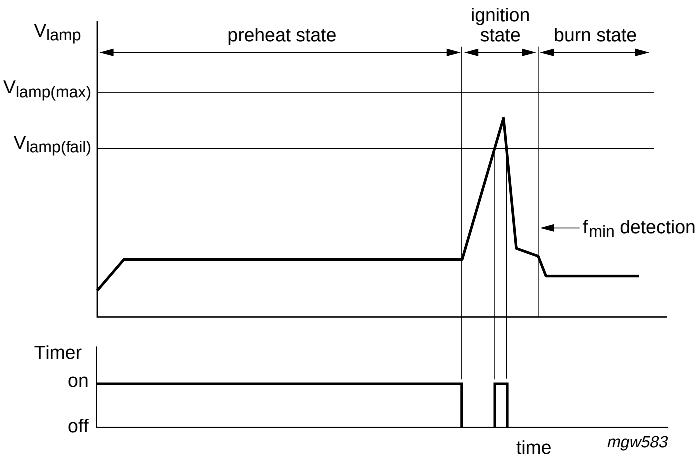


Fig 5. Normal ignition behavior

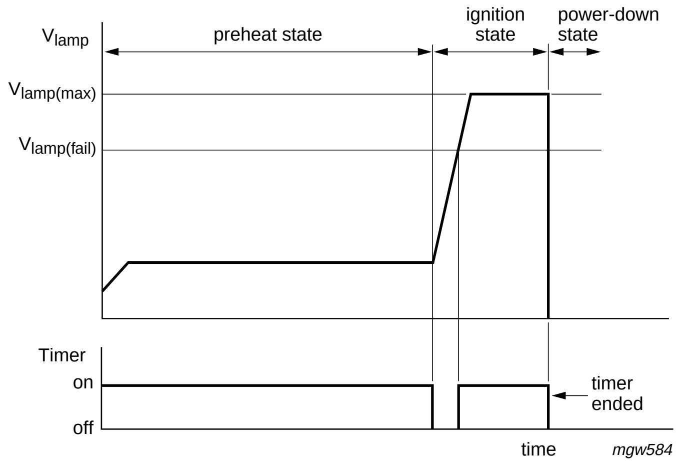


Fig 6. Failure mode during ignition

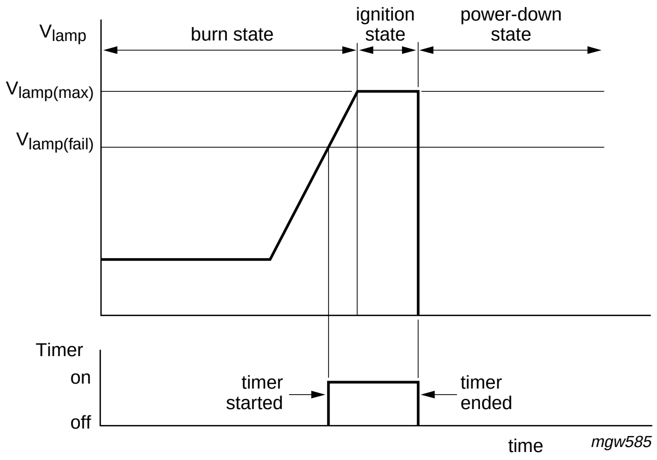


Fig 7. Failure mode during burn

9. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{HS}	high-side supply voltage	I_{HS} < 30 µA; t < 1 s	-	600	V
		I_{HS} < 30 µA	-	510	V
V_{DD}	voltage at pin V_{DD}		-	14	V
V_{ACM}	voltage at pin ACM		–5	+5	V
V_{PCS}	voltage at pin PCS		–5	+5	V
V_{LVS}	voltage at pin LVS		0	5	V
V_{CSP}	voltage at pin CSP		0	5	V
V_{CSN}	voltage at pin CSN		–0.3	+5	V
V_{CSW}	voltage at pin CSW		0	5	V
T_{amb}	ambient temperature		–25	+80	°C
T_j	junction temperature		–25	+150	°C
T_{stg}	storage temperature		–55	+150	°C
V_{esd}	electrostatic discharge voltage				
	pins FV_{DD}, GH and SH	[1]	–1000	+1000	V
	pins CT, CSW, CF, IREF, GL, V_{DD}, PCS, CSN, CSP, VREF, LVS and ACM	[1]	–2500	+2500	V

[1] In accordance with the human body model, i.e. equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

10. Thermal characteristics

Table 5: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	SO16		100	K/W
	DIP16		60	K/W
$R_{th(j-pin)}$	thermal resistance from junction to pin	in free air		
	SO16		50	K/W
	DIP16		30	K/W

11. Characteristics

Table 6: Characteristics
V_{DD} = 13 V; $V_{FVDD} - V_{SH}$ = 13 V; T_{amb} = 25 °C; all voltages referenced to GND; see test circuit of Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up state: pin V_{DD}						
V_{DD}	supply voltage for defined driver output	TR1 = off; TR2 = off	-	-	6	V
$V_{DD(reset)}$	reset supply voltage	TR1 = off; TR2 = off	4.5	5.5	7.0	V
$V_{DD(stop)}$	oscillator stop supply voltage		8.6	9.1	9.6	V
$V_{DD(start)}$	oscillator start supply voltage		12.4	13.0	13.6	V
$V_{DD(hys)}$	start-stop hysteresis supply voltage		3.5	3.9	4.4	V
$V_{DD(clamp)}$	clamp supply voltage	Power-down mode	10	11	12	V
$I_{DD(start)}$	start-up supply current	$V_{DD} < V_{DD(start)}$	-	170	200	µA
$I_{DD(pd)}$	power-down supply current	V_{DD} = 9 V	-	170	200	µA
I_{DD}	operating supply current	f_{bridge} = 40 kHz without gate drive	-	1.5	2.2	mA
High-voltage supply: pins GH, SH and FV_{DD}						
I_L	leakage current	600 V at high-voltage pins	-	-	30	µA
Reference voltage: pin VREF						
V_{VREF}	reference voltage	I_L = 10 µA	2.86	2.95	3.04	V
ΔV_{VREF}	reference voltage stability	I_L = 10 µA; T_{amb} = 25 °C to 150 °C	-	–0.64	-	%
I_{source}	source current		1	-	-	mA
I_{sink}	sink current		1	-	-	mA
Z_o	output impedance	I_L = 1 mA source	-	3.0	-	Ω
Current supply: pin IREF						
V_I	input voltage		-	2.5	-	V
I_I	reference input current range		65	-	95	µA
Voltage controlled oscillator						
Output: pin CSW						
V_o	output control voltage		2.7	3.0	3.3	V
V_{clamp}	clamp voltage	burn state	2.8	3.1	3.4	V
Voltage controlled oscillator output: pin CF						
f_{max}	maximum bridge frequency		90	100	110	kHz
f_{min}	minimum bridge frequency		38.9	40.5	42.1	kHz
Δf_{stab}	frequency stability	T_{amb} = –20 °C to +80 °C	-	1.3	-	%
t_{start}	first output oscillator stroke time		-	50	-	µs
$t_{no(min)}$	minimum non-overlap time	GH to GL	0.68	0.90	1.13	µs
		GL to GH	0.75	1.00	1.25	µs
$t_{no(max)}$	maximum non-overlap time	f_{bridge} = 40 kHz [1]	-	7.5	-	µs
$V_{CF(high)}$	high-level oscillator output voltage	$f = f_{min}$	-	2.5	-	V

Table 6: Characteristics *…continued*

V_{DD} = 13 V; $V_{FVDD} - V_{SH}$ = 13 V; T_{amb} = 25 °C; all voltages referenced to GND; see test circuit of Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{o(start)}$	oscillator output start current	V_{CF} = 1.5 V	3.8	4.5	5.2	µA
$I_{o(min)}$	minimum oscillator output current	V_{CF} = 1.5 V	-	21	-	µA
$I_{o(max)}$	maximum oscillator output current	V_{CF} = 1.5 V	-	54	-	µA
Output drivers						
High-side driver output: pin GH						
V_{OH}	HIGH-level output voltage	I_o = 10 mA	12.5	-	-	V
V_{OL}	LOW-level output voltage	I_o = 10 mA	-	-	0.5	V
$I_{o(source)}$	output source current	$V_{GH} - V_{SH}$ = 0 V	135	180	235	mA
$I_{o(sink)}$	output sink current	$V_{GH} - V_{SH}$ = 13 V	265	330	415	mA
R_{on}	on resistance	I_o = 10 mA	32	39	45	Ω
R_{off}	off resistance	I_o = 10 mA	16	21	26	Ω
Low-side driver output: pin GL						
V_{OH}	HIGH-level output voltage	I_o = 10 mA	12.5	-	-	V
V_{OL}	LOW-level output voltage	I_o = 10 mA	-	-	0.5	V
$I_{o(source)}$	output source current	V_{GL} = 0	135	200	235	mA
$I_{o(sink)}$	output sink current	V_{GL} = 13 V	265	330	415	mA
R_{on}	on resistance	I_o = 10 mA	32	39	45	Ω
R_{off}	off resistance	I_o = 10 mA	16	21	26	Ω
Floating supply voltage: pin FV_{DD}						
V_{FVDD}	lockout voltage		2.8	3.5	4.2	V
I_{FVDD}	floating well supply current	DC level at $V_{GH} - V_{SH}$ = 13 V	-	35	-	µA
Bootstrap diode						
V_{boot}	bootstrap diode forward drop voltage	I = 5 mA	1.3	1.7	2.1	V
Preheat current sensor						
Input: pin PCS						
I_i	input current	V_{PCS} = 0.6 V	-	-	1	µA
V_{ph}	preheat voltage		0.57	0.60	0.63	V
Output: pin CSW						
$I_{o(source)}$	output source current	V_{CSW} = 2.0 V	9.0	10	11	µA
$I_{o(sink)}$	output sink current	V_{CSW} = 2.0 V	-	10	-	µA
Adaptive non-overlap and capacitive mode detection; pin ACM						
I_i	input current	V_{ACM} = 0.6 V	-	-	1	µA
V_{CMDP}	positive capacitive mode detection voltage		80	100	120	mV
V_{CMDN}	negative capacitive mode detection voltage		–68	–85	–102	mV

Table 6: Characteristics *…continued*

V_{DD} = 13 V; V_{FVDD} – V_{SH} = 13 V; T_{amb} = 25 °C; all voltages referenced to GND; see test circuit of Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Lamp voltage sensor						
Input: pin LVS						
I_i	input current	V_{LVS} = 0.81 V	-	-	1	µA
$V_{lamp(fail)}$	lamp fail voltage		0.77	0.81	0.85	V
$V_{lamp(fail)(hys)}$	lamp fail hysteresis voltage		119	144	169	mV
$V_{lamp(max)}$	maximum lamp voltage		1.44	1.49	1.54	V
Output: pin CSW						
$I_{o(sink)}$	output sink current	V_{CSW} = 2.0 V	27	30	33	µA
$I_{o(source)}$	ignition output source current	V_{CSW} = 2.0 V	9.0	10	11	µA
Average current sensor						
Input: pins CSP and CSN						
I_i	input current	V_{CS} = 0 V	-	-	1	µA
V_{offset}	offset voltage	V_{CSP} = V_{CSN} = 0 V to 2.5 V	–2	0	+2	mV
g_m	transconductance	f = 1 kHz	1900	3800	5700	µA/mV
Output: pin CSW						
I_o	output current	source and sink; V_{CSW} = 2 V	85	95	105	µA
Preheat timer; pin CT						
t_{ph}	preheat time	C_{CT} = 330 nF; R_{IREF} = 33 kΩ	1.6	1.8	2.0	s
t_{ign}	ignition time	C_{CT} = 330 nF; R_{IREF} = 33 kΩ	-	0.32	-	s
I_o	output current	V_{CT} = 2.5 V	5.5	5.9	6.3	µA
V_{OL}	LOW-level output voltage		-	1.4	-	V
V_{OH}	HIGH-level output voltage		-	3.6	-	V
V_{hys}	output hysteresis voltage		2.05	2.20	2.35	V

[1] The maximum non-overlap time is determined by the level of the CF signal. If this signal exceeds a level of 1.25 V, the non-overlap will end, resulting in a maximum non-overlap time of 7.5 µs at a bridge frequency of 40 kHz.

12. Application information

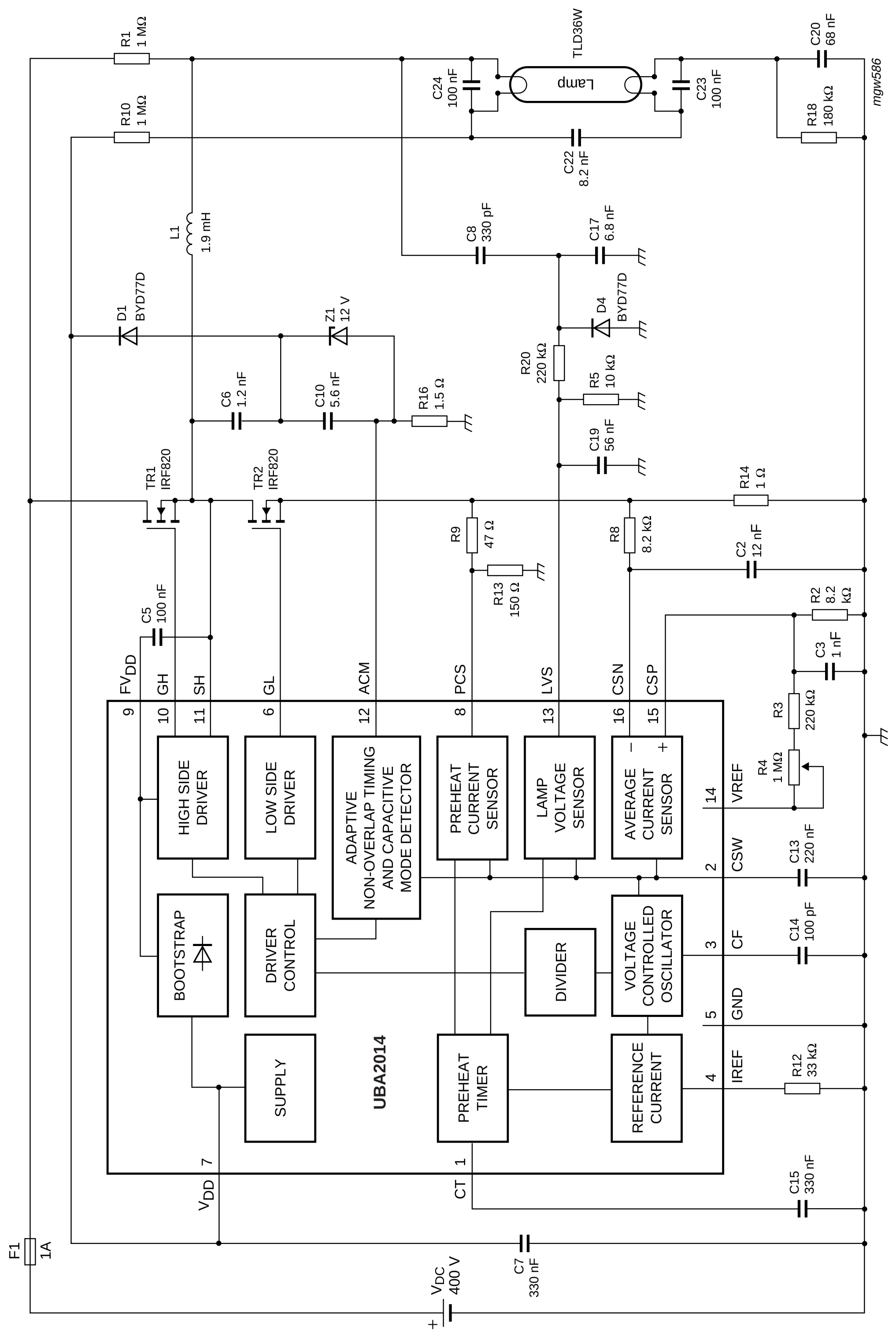


Fig 8. Test and application circuit

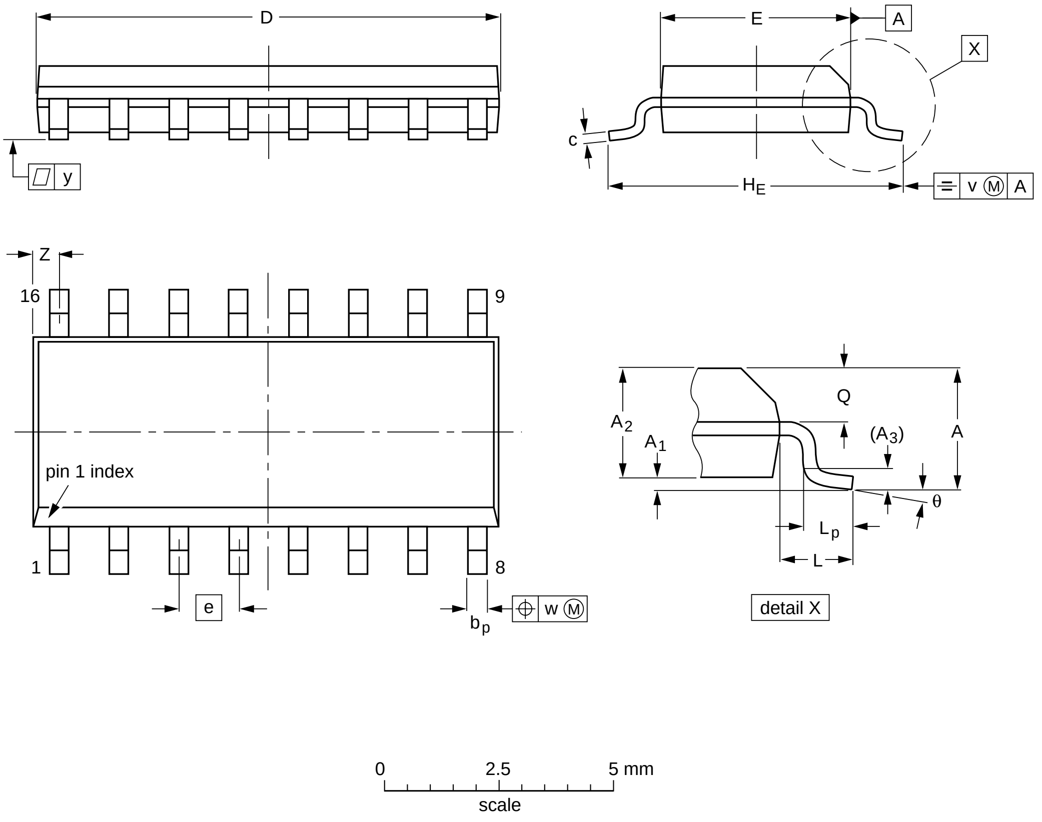
13. Test information

13.1 Quality information

The *General Quality Specification for Integrated Circuits, SNW-FQ-611* is applicable.

14. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

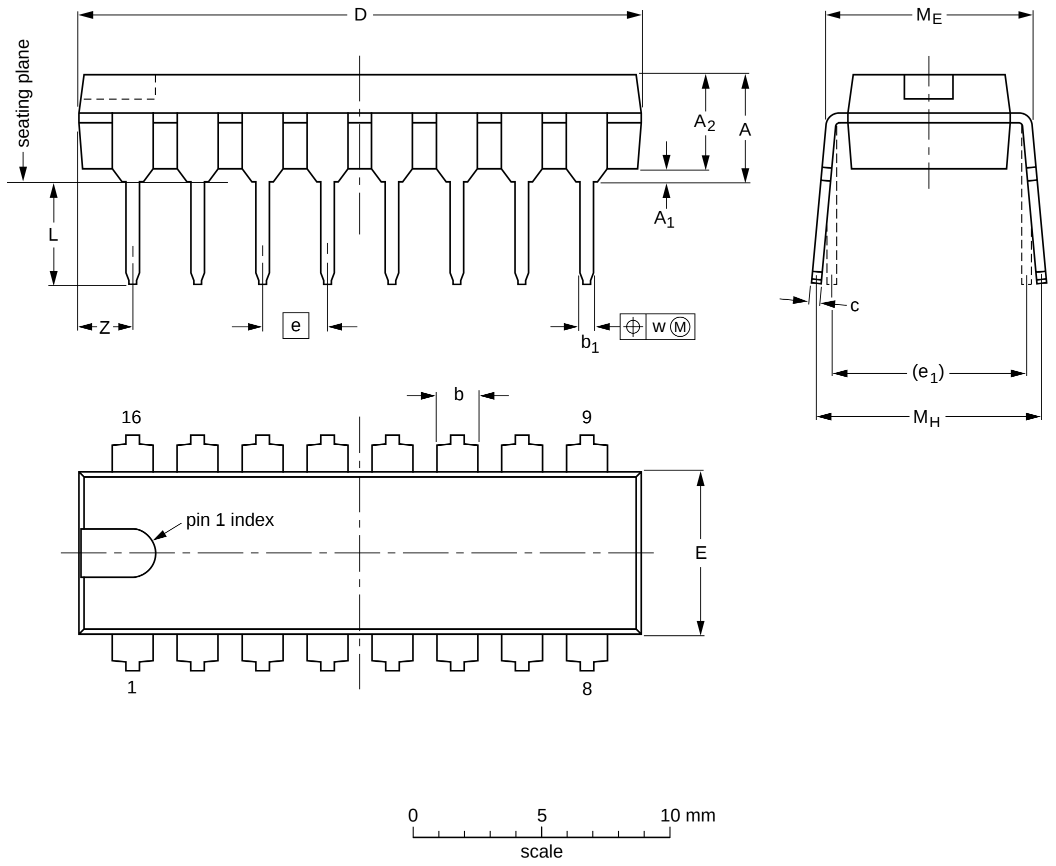
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT109-1 (SO16)

DIP16: plastic dual in-line package; 16 leads (300 mil); long body SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.02	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.1	0.3	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-1	050G09	MO-001	SC-503-16			~~99-12-27~~ 03-02-13

Fig 10. Package outline SOT38-1 (DIP16)

15. Soldering

15.1 Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

15.2 Through-hole mount packages

15.2.1 Soldering by dipping or by solder wave

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

15.2.2 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 °C and 400 °C, contact may be up to 5 seconds.

15.3 Surface mount packages

15.3.1 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages

  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

15.3.2 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.3.3 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

15.4 Package related soldering information

Table 7: Suitability of IC packages for wave, reflow and dipping soldering methods

Mounting	**Package** [1]	**Soldering method**		
		Wave	**Reflow** [2]	**Dipping**
Through-hole mount	CPGA, HCPGA	suitable	–	–
	DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable [3]	–	suitable
Through-hole-surface mount	PMFP [4]	not suitable	not suitable	–
Surface mount	BGA, HTSSON..T [5], LBGA, LFBGA, SQFP, SSOP..T [5], TFBGA, VFBGA, XSON	not suitable	suitable	–
	DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [6]	suitable	–
	PLCC [7], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended [7] [8]	suitable	–
	SSOP, TSSOP, VSO, VSSOP	not recommended [9]	suitable	–
	CWQCCN..L [10], WQCCN..L [10]	not suitable	not suitable	–

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods.*

[3] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[4] Hot bar soldering or manual soldering is suitable for PMFP packages.

[5] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[6] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[7] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[8] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[9] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[10] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

16. Revision history

Table 8: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
UBA2014_2	20050912	Product data sheet	-	9397 750 11428	UBA2014_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • DIP16 package added • Change to design equations				
UBA2014_1	20020516	Product specification	-	9397 750 09094	-

17. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

18. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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22. Contents

Date of release: 12 September 2005
Document number: 9397 750 11428

Published in The Netherlands